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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR:	Haswell et al.	EXAMINER:	Mujtaba M. Chaudry
SERIAL NO.:	10/604,141	ART UNIT:	2133
FILING DATE:	June 27, 2003	DATE:	November 20, 2006
FOR:	Method and System for Optimized Instruction Fetch to Protect Against Soft and Hard Errors		

RESPONSE AFTER FINAL

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is responsive to the Office Action mailed September 19, 2006 finally rejecting the instant application.

Claims 1-20 stand finally rejected under 35 USC § 103 as being obvious from Sakamoto U.S. Patent No. 4,617,660 in view of Albonesi U.S. Patent No. 4,920,539. Applicants again respectfully traverse this rejection.

The Examiner continues to correctly state that "Sakamoto does not explicitly teach to check the data signal for corruption at the time it is received by the computer processor as stated in the present application." Office action, p.5. However, not only does Sakamoto not